REMARKS

The Applicant appreciates the time taken by the Examiner to review the Applicant's present application. This application has been carefully reviewed in light of the Examiner's comments, including the Office Action mailed August 7, 2007. The Applicant respectfully requests reconsideration and favorable action in this case.

Summary of rejections and amendments

The Examiner rejected claims 1-21 under 35 U.S.C. 103. The Applicant has not amended any of the claims. Claims 1-21 are therefore pending in the application.

Rejections under 35 U.S.C. §103

Claims 1, 3, 8, 11, 15 and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,765,931 ("Rabenko") in view of U.S. Patent No. 6,044,113 ("Oltean"). Claims 2, 12 and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Rabenko in view of Oltean and further in view of U.S. Patent Application Pub. No. 2003/0037297 ("Araki"). Claims 9 and 16 are rejected under 35 U.S.C. §103(a) as being unpatentable over Rabenko in view of Oltean and further in view of U.S. Patent No. 5,367,162 ("Holland"). Claims 4 and 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Rabenko in view of Oltean and further in view of U.S. Patent No. 6,393,198 ("LaMacchia"). Claims 5, 6, 7 and 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Rabenko in view of Oltean and further in view of U.S. Patent No. 5,621,805 ("Loh"). Claims 20 and 21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Rabenko in view of Oltean and further in view of U.S. Patent No. 6,665,338 ("Midya"). Claims 10 and 17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Rabenko in view of Oltean and further in view of Holland and Loh. The Applicant respectfully traverses these rejections. Claim 1 is exemplary and will be discussed in detail below.

Requirements to establish obviousness

In order to establish a prima facie case of obviousness in accordance with M.P.E.P. 2143, it is necessary to meet three criteria. The prior art references must teach or suggest all the claim limitations, there must be some suggestion or motivation to modify the references or to combine reference teachings, and there must be a reasonable expectation of success. The Applicant respectfully submits that these criteria have not been met, and that a prima facie case of obviousness has not been established. Claim 1 is exemplary of the claims pending in the

application and will be discussed in detail below in regard to the shortcomings of the cited references.

The references do not disclose all of the claim limitations

The Examiner states that Rabenko teaches first and second counters coupled to receive the clock signal from the clock source, where the first counter counts cycles of the clock signal in the sample period corresponding to a first digital data stream and the second counter also counts cycles of the clock signal (citing figure 17, elements 556-558 and 560, and, lines 14-24.) The Examiner states that Rabenko does not teach that the second counter counts cycles of the clock signal in a sample period corresponding to a second digital data stream, but asserts that this is taught by Oltean at col. 1, lines 21-48, and in figure 1, elements 102, 106(a) and 106(b). The Applicant respectfully disagrees.

While both Rabenko and Oltean each include two counters, neither of the references teaches that the counters are configured to count the number of cycles of the received clock signal in the sample period at a corresponding data stream. In the case of Rabenko, each of counters 556 and 557 receives a pair of clock signals -- the 24.576MHz reference clock signal and an 8kHz clock signal (either ADC clock 556 or TRC clock 558.) The purpose of these counters is to determine differences between the 8kHz ADC and TRC clock signals in order to prevent data overflow (col. 29, lines 40-58.) Neither of these counters counts the number of clock cycles in a sample period of the data stream (which is shown in figure 17 as being provided to sampling-rate tracker algorithm 554,) so neither of the counters meets the limitations of claim 1. In the case of Oltean, each of counters 106(a) and 106(b) is loaded by processor 104 with a value (N1 or N, respectively) corresponding to a rising or falling edge of a PWM pulse. Neither of these counters counts the number of clock cycles in a sample period of a data stream so, again, neither of the counters meets the limitations of claim 1.

No motivation to combine references

As noted above, M.P.E.P. 2143 requires that the prior art must contain some suggestion or motivation to modify the references or to combine reference teachings. This teaching, suggestion or motivation must be found in the references themselves, or in the knowledge generally available to one of ordinary skill in the art.

The Examiner asserts that a person of ordinary skill would be motivated to combine the disclosure of Oltean with that of Rabenko in order to produce a precise and stable duty cycle for providing control to complex electronic devices as taught by Oltean. The Applicant respectfully submits that the Rabenko and Oltean references provide no such motivation. The Applicant points out that Rabenko does not provide any indication of a need for a precise or stable duty

cycle. Duty cycles are not discussed in Rabenko, and the term "duty cycle" does not even appear in the reference. It is therefore apparent that a person of ordinary skill in the art would not be motivated to combine the references to produce a precise and stable duty cycle as suggested by the Examiner.

No reasonable expectation of success

Even if there were some motivation or suggestion to combine the references, the Applicant further respectfully submits that a person of ordinary skill would not have a reasonable expectation of success in combining the teachings of the two references. As explained above, Rabenko uses the two counters (556, 557) to account for differences between the 8kHz ADC clock signal and the 8kHz TRC clock signal and thereby avoid data overflows. It is not apparent how the teachings of Oltean, i.e., counters which modulo-count clock cycles up to specific numbers which are loaded into the counters by a processor, would be incorporated into the device of Rabenko, since the counters of the two references are intended to perform entirely different functions, i.e., accounting for clock signal mismatches (Rabenko) and defining rising/falling edges of PWM pulses (Oltean.) Even if the present disclosure could be used as a roadmap for the combination of the Rabenko and Oltean references' teachings (which is impermissible under M.P.E.P. 2143.01,) the distinct purposes and structures of the respective devices make it unlikely that they could be combined to arrive at the recited invention.

No prima facie case of obviousness has been established

As explained above, the Examiner has failed to show that the Rabenko and Oltean references disclose all of the limitations of claim 1, that the references themselves or the teaching generally available in the art provide some motivation to combine the references, and that a person of ordinary skill would have a reasonable expectation of success in combining the references to arrive at the invention. Consequently, the Examiner has failed to make a prima facie case of obviousness of claim 1 as required by M.P.E.P. 2143. The Applicant therefore respectfully requests that the rejection of claim 1 under 35 U.S.C. §103(a) be withdrawn.

Additional claims

Because claims 2-21 include limitations similar to those of claim 1, and because these claims are rejected at least in part based on the combination of Rabenko and Oltean, the Examiner has failed to meet his burden to under M.P.E.P. 2143 as to claims 2-21. The Applicant therefore respectfully requests that the rejections of these claims under 35 U.S.C. §103(a) be withdrawn as well.

The Applicant points out that, in addition to the failure of the cited references to teach the limitations discussed above, the dependent claims in the application include additional

limitations that are not taught or suggested by the references. For instance, claims 8 and 15 recite limitations as to the estimation of a sample rate of the first data stream and determination of a sample rate estimate for the second data stream based on the ratio of the first and second numbers of cycles counted by the counters. Rabenko teaches that counters 556 and 557 are used to determine differences between the 8kHz ADC clock signal and the 8kHz TRC clock signal. Oltean teaches that the counter values loaded into the counters are used to generate rising and falling edges of a PWM pulse. No sample rate estimation is performed for any data streams, and there certainly is no estimation of a second data stream's sample rate based on a ratio of counter values. Claims 8 and 15 are therefore further distinguished from Rabenko and Oltean.

Claims 2, 12 and 13 include limitations regarding incrementing each counter once for each cycle after a frame sync signal is received in the corresponding data stream. The Examiner asserts that this limitation is taught by Araki. Araki, however, clearly teaches that the disclosed counters are frame counters which are incremented once for each received frame (or frame sync signal,) rather than once for each cycle after the frame sync signal is received. According to this teaching, each counter would be incremented once during each sample period, and would retain this value throughout the sample period rather than counting the clock cycles during the sample period. This is substantially different than the recited limitations of claims 2, 12 and 13, so these claims are further distinguished from Rabenko, Oltean and Araki.

Claims 4 and 14 recite limitations as to resetting the counters each time a frame sync signal is received. The Examiner asserts that this limitation is taught by LaMacchia (citing Figure 3, elements 42, 114, 116; col. 12, line 62 through col. 13, line 1; col. 13, lines 10-22 and col. 17, lines 35-47.) These portions of LaMacchia, however, do not teach the resetting of counters when frame sync signals are received. Instead, the cited portions of LaMacchia teach that a counter is reset by a command from a digital audio workstation, or DAW (col. 12, line 62 through col. 13, line 1 and col. 13, lines 10-22,) and that the counter may be reset at a specified time in the future (col. 17, lines 35-47.) LaMacchia specifically states that this future reset is at least two frames after the current time (col. 17, line 34,) so it is necessarily true that the counter will not be reset when a frame sync signal (e.g., the frame sync signal between frames 1 and 2) is received. LaMacchia therefore actually teaches away from the limitations recited in claims 4 and 14, so these claims are further distinguished from Rabenko, Oltean and LaMacchia.

In addition to the failure of the cited references to disclose the claims limitations as suggested by the Examiner, the Applicant points out that a person of ordinary skill would not be motivated to combine the additional references with Rabenko and Oltean as suggested by the

Examiner. For example, the Examiner suggests that a person of ordinary skill would be motivated to combine Araki with Rabenko and Oltean "in order to establish frame synchronization as taught by Araki." It is not apparent how including the frame synchronization of Araki in the systems of Rabenko and/or Oltean would result in the counting of clock cycles following receipt of the frame sync signals (as recited in claims 2, 12 and 13,) since this is not required for frame synchronization. It is only when the disclosure of the present application is used as a roadmap that the person of ordinary skill is able to reconstruct the claimed invention from the disparate bits and pieces gleaned from Rabenko, Oltean and Araki. As noted above, such hindsight reconstruction of the invention from the references is impermissible under M.P.E.P. 2143.01. Similarly, the Examiner suggests that a person of ordinary skill would be motivated to combine LaMacchia with Rabenko and Oltean "in order to reset counters at the digital workstation (digital system) because counters are accurately aligned, trigger positions without introducing variable delays in the digital system which is inherent in software triggering". The invention, however, has nothing to do with variable delays in software triggering or alignment of counters or trigger positions. The motivations suggested by the Examiner therefore would not lead a person of ordinary skill to reconstruct the invention from separate pieces of the references which have very different functions from the invention.

The Applicant also points out that the references cited with respect to the dependent claims fail not only to disclose the limitations of the dependent claims, but also fail to remedy the deficiencies of Rabenko and Oltean as explained above. Consequently, the cited references, including the possible combinations of Rabenko, Oltean, Araki, Holland, LaMacchia, Loh and Midya, fail to render even the independent claims of the application obvious.

Conclusion

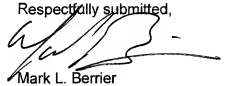
The Applicant has now made an earnest attempt to place this case in condition for allowance. Other than as explicitly set forth above, this reply does not include an acquiescence to statements, assertions, assumptions, conclusions, or any combination thereof in the Office Action.

For at least the foregoing reasons, the Applicant respectfully requests allowance of all claims pending in the application. The Examiner is invited to telephone the undersigned at the number listed below for prompt action in the event any issues remain.

If any extensions of time are necessary to prevent the above referenced application from becoming abandoned, the Applicant hereby petitions for such extensions. If any fees are inadvertently omitted, or if any additional fees are required, or if any amounts have been

overpaid, please appropriately charge or credit those fees to Deposit Account No. 50-3085 of the Law Offices of Mark L. Berrier.

Respectfully submitted,



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